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EXAMINER	
VITAL, PIERRE M	
ART UNIT	PAPER NUMBER
2188	10

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/922,153	Applicant(s) MORAN, DOV	
	Examiner Pierre M. Vital	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed July 3, 2003 in response to PTO Office Action mailed May 7, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-28 have been presented for examination in this application. In response to the last Office Action, claims 1, 12 and 18-23 have been amended. Claim 2 has been canceled. Claims 24-28 have been added. As a result, claims 1, 3-28 are now pending in this application.

3. The objection to the drawings as in the Office Action mailed May 7, 2003 (Paper No. 6) is respectfully maintained and reiterated below for applicant's convenience.

Drawings

4. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

> All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the manner of a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings and **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 10, 12-13, 16, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Kakinuma et al (US5,640,349).

As per claims 1, 12, 18, 20 and 21, Brown discloses a flash-based unit for providing code to be executed by an external processor that is in communication with the flash based unit by a bus, the flash based unit comprising a flash memory for storing the code to be executed [*flash EPROM stores both code and data;* col. 9, line 50], said flash memory being of a type such that the code cannot be executed in place from said flash memory [*although a flash EPROM is used, NAND flash may be used as well;* col. 5, lines 30-33]; a volatile memory component for receiving at least a portion of the code to be executed, such that at least said portion of the code is executed by the external processor from said volatile memory component [*the code of the flash memory is copied to volatile memory where the processor can satisfy the code fetch request;* col. 4, lines 4-8].

However, Brown does not specifically teach a logic, separate from the external processor, for receiving command to move said at least portion of the code from said flash memory to said volatile memory component as recited in the claims.

Kakinuma discloses a logic, separate from the external processor, for receiving command to move said at least portion of the code from said flash memory to said volatile memory component [*flash memory controller 2 controls read/write to/from flash memory based on command by host computer*; Fig. 1A, 1B, col. 1, line 35 – col. 2, line 3].

It would have been obvious to one of ordinary skill in the art, having the teachings of Brown and Kakinuma before him at the time the invention was made, to modify the system of Brown to include a logic, separate from the external processor, for receiving command to move said at least portion of the code from said flash memory to said volatile memory component because it would have provided improved system throughput by providing an external buffer memory which receives a plurality of sectors from a host computer simultaneously [col. 2, lines 48-51] as taught by Kakinuma.

As per claims 10 and 16, Brown discloses a volatile memory component selected from the group consisting of SRAM or DRAM [col. 4, lines 1-3].

As per claim 13, Brown discloses a restricted non-volatile memory is a flash memory [col. 5, lines 30-32].

7. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Anderson et al (US6,295,577).

As per claim 3, Brown discloses the claimed invention as detailed above in the previous paragraphs. However, Brown does not specifically teach a power storage for storing at least a limited amount of power for supplying power to the flash-based unit if power is not otherwise available, power being drawn form said power storage when said logic determines that said power is not otherwise available as recited in the claim.

Anderson discloses a power storage for storing at least a limited amount of power for supplying power to the flash-based unit if power is not otherwise available, power being drawn form said power storage when said logic determines that said power is not otherwise available [*power is supplied to the non-volatile memory upon loss of power;* col. 6, lines 2-6].

As per claim 4, Brown discloses the claimed invention as detailed above in the previous paragraphs. However, Brown does not specifically teach a power storage providing only sufficient power to write data in said volatile memory to said flash memory as recited in the claim.

Anderson discloses a power storage providing only sufficient power to write data in said volatile memory to said flash memory [*data is stored from volatile memory to non-volatile memory upon detection of loss of power;* col. 5, lines 61-67].

As per claim 5, Brown discloses the claimed invention as detailed above in the previous paragraphs. However, Brown does not specifically teach the power storage is a capacitor as recited in the claim.

Anderson discloses the power storage is a capacitor [col. 3, lines 62-63].

It would have been obvious to one of ordinary skill in the art, having the teachings of Brown and Anderson before him at the time the invention was made, to modify the system of Brown to include a power storage for storing at least a limited amount of power for supplying power to the flash-based unit if power is not otherwise available, power being drawn form said power storage when said logic determines that said power is not otherwise available; a power storage providing only sufficient power to write data in said volatile memory to said flash memory and the power storage is a capacitor because it would have decreased system cost by using a back EMF to power the non-volatile memory rather than battery based systems [col. 5, lines 10-14] as taught by Anderson.

8. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Mills et al (US6,385,688).

As per claims 6 and 7, Brown discloses the claimed invention as detailed above in the previous paragraphs. However, Brown does not specifically teach a single chip or die for containing all components of a flash based unit as recited in the claims.

Mills discloses a single chip or die for containing all components of a flash based unit [col. 20, lines 1-4].

It would have been obvious to one of ordinary skill in the art, having the teachings of Brown and Mills before him at the time the invention was made, to modify the system of Brown to include a single chip or die for containing all components of a flash based unit because it would have improved system performance by reducing or eliminating the lengthy process of obtaining information from disk when power is turned on [col. 9, lines 15-20] as taught by Mills.

9. Claims 8-9 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Nakata (US6,523,101).

As per claims 8 and 14, Brown discloses the claimed invention as detailed above in the previous paragraphs. However, Brown does not specifically teach a flash memory only permitting data to be read in one or more specific sizes of blocks as recited in the claim.

Nakata discloses a flash memory only permitting data to be read in one or more specific sizes of blocks [*ROM indicates copy size of initialization data to be stored into RAM;* col. 3, lines 41-44].

It would have been obvious to one of ordinary skill in the art, having the teachings of Brown and Nakata before him at the time the invention was made, to modify the system of to include a flash memory only permitting data to be read in one or more specific sizes of blocks because it would have increased execution speed of the

program by allowing the text codes stored on the ROM to be copied once into the RAM [col. 1, lines 43-46] as taught by Nakata.

As per claims 9 and 15, Brown discloses a flash memory is a NAND-type flash memory [*although a flash EPROM is used, NAND flash may be used as well;* col. 5, lines 30-33].

10. Claims 11, 17, 19 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Esfahani et al (US6,434,695).

As per claims 11, 17, 19 and 22, Brown discloses the claimed invention as detailed above in the previous paragraphs. However, Brown does not specifically teach executing the portion of the code to boot the system and that said portion of the boot code being for basic initialization of the system as recited in the claims.

Esfahani discloses executing the portion of the code to boot the system [*compressed image of the first portion of the OS is executed as part of the boot sequence of the computer system*; col. 2, lines 6-12]; and that said portion of the boot code being for basic initialization of the system [*RTAS is instantiated in RAM*; col. 7, lines 2-4].

It would have been obvious to one of ordinary skill in the art, having the teachings of Brown and Esfahani before him at the time the invention was made, to modify the system of Brown to include executing the portion of the code to boot the system and that said portion of the boot code being for basic initialization of the system because it would have provided increased reliability in the system by allowing run-time

checks determining which hardware to initialize and which code to execute and install instead of having only the correct code built in [col. 10, lines 48-50] as taught by Esfahani.

As per claim 23, Esfahani discloses transferring a second portion of the code to said volatile memory component for booting the system [col. 13, lines 23-24].

11. Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Esfahani et al (US6,434,695) and further in view of Mahmoud (US6,567,911).

As per claims 24-28, the combination of Brown and Esfahani discloses the claimed invention as detailed above in the previous paragraphs. However, Brown and Esfahani do not specifically teach that the volatile memory is large enough to store portion of the boot code only sufficient for basic initialization of a system as recited in the claims.

Mahmoud discloses the use of a volatile memory is large enough to store at least portion of a boot code only sufficient for basic initialization of a system [*RAM has a confined size for accommodating at least a portion of BIOS image*; col. 3, lines 16-18].

It would have been obvious to one of ordinary skill in the art, having the teachings of Brown and Esfahani and Mahmoud before him at the time the invention was made, to modify the system of Brown and Esfahani to include the use of a volatile

memory is large enough to store at least portion of a boot code only sufficient for basic initialization of a system because it would have provided an improved conservation of memory resources available to a computer system during execution of the system BIOS by reducing the amount of memory area that is occupied by the system's various BIOS images [col. 2, lines 17-23] as taught by Mahmoud.

Response to Arguments

12. Applicant's arguments with respect to claims 1 and 3-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach transferring code to be executed from flash memory to volatile; executing said code from volatile memory by a processor and utilizing logic other than processor to move code from flash to volatile memory and the use of a volatile memory is large enough to store at least portion of a boot code only sufficient for basic initialization of a system.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Mano Padmanabhan
9/8/03

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 2100

Pierre M. Vital
September 8, 2003